Exhibit 37

IN THE UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
WACO DIVISION

ACQIS LLC, a Texas limited liability company Plaintiff, v. MICROSOFT CORPORATION, a Washington corporation. Defendant.	§ § § § § § § § § §	Civil Action No. 6:22-cv-385-ADA **JURY TRIAL DEMANDED**

ACQIS LLC, a Texas limited liability company Plaintiff, v. SONY INTERACTIVE ENTERTAINMENT INC., a Japanese corporation, and SONY INTERACTIVE ENTERTAINMENT LLC, a California limited liability corporation. Defendants.	§ § § § § § § § § §	Civil Action No. 6:22-cv-386 **JURY TRIAL DEMANDED**

DECLARATION OF ROBERT P. COLWELL, PH.D. IN SUPPORT OF DEFENDANTS' CONSOLIDATED OPENING CLAIM CONSTRUCTION BRIEF

I, Robert P. Colwell, Ph.D., declare as follows:

I. Background and Qualifications

1. I submit this declaration in support of Microsoft's, Sony Interactive Entertainment LLC's and Sony Interactive Entertainment Inc.'s (collectively, "Defendants") proposed claim constructions concerning U.S. patent nos. 8,977,797 ("'797 patent"); 9,529,768 ("'768 patent"); 9,703,750 ("'750 patent"); RE44,654 ("'654 patent") and RE45,140 ("'140 patent") (collectively "the Asserted Patents").

2. I am being compensated for my time at my standard consulting rate. My compensation is in no way contingent on the results of this litigation.

3. My complete qualifications and professional experience are described in my curriculum vitae, a copy of which is attached as Appendix A. The following is a brief summary of my relevant qualifications and professional experience.

4. I have nearly 40 years of professional experience in the field of processor and system architecture design. I am an expert in, among other things, CPU architecture and computer systems.

5. I received an undergraduate Bachelor of Science degree in Electrical Engineering from the University of Pittsburgh in 1977. I received a MS degree in Computer Engineering in 1978 as well as a Ph.D. in Computer Engineering in 1985, both from Carnegie-Mellon University.

6. I have been working in the field of computer engineering and, in particular, microprocessor and multiprocessor design, since 1977. This includes work at Bell Telephone Laboratories (1977-1980), Three Rivers Computer (1980-1985), Multiflow Computer (1985-1990), and Intel Corporation (1990-2001). I have remained active in the field as an author, lecturer, consultant and technical expert in litigation.

7. From 1990-1992, I held the position of Senior CPU Architect in which I was one of just three senior architects responsible for designing Intel's P6 microarchitecture that is the core of Intel's Pentium II, Pentium III, Celeron, Xeon and Centrino families of CPUs (Central Processing Units). From 1992-2001, I held the position of Chief IA-32 Architect, in which I was responsible for all of Intel's Pentium CPU architecture efforts and initiated and led Intel's Pentium 4 CPU core development.

8. From 1977 to 1980, I held an engineering position at Bell Telephone Laboratories where I worked on, among other things, microprocessor hardware design.

9. From 1980 to 1984, I held the position of Hardware Engineer at Perq Systems Corp. on a part-time basis from 1980-1984 while I was working on my Ph.D. I was a hardware design engineer for graphics display hardware for first generation bit-slice-based engineering workstations.

10. From 1985-1990, I held the position of Hardware Architect at Multiflow Computer, Inc. I was one of only seven hardware designers who created the world's first VLIW (Very Long Instruction Word) scientific supercomputer.

11. I became a self-employed industry consultant in 2001, working with computer industry clients such as Safeware, the University of Pittsburgh, Intel, Qualcomm, Lawrence Berkeley National Labs, venture capital companies, and the U.S. Department of Defense (DoD).

12. From 2011 to 2014, I worked at Defense Advanced Research Projects Agency (DARPA) first as Deputy Director, then Director, of the Microsystems Technology Office (MTO). MTO had an annual budget of approximately $600M, and my job as office leader was to invest that money in promising new technologies for the DoD, including new energy-efficient computing systems, modular and adaptable radars, position/navigation/timing systems for GPS-denied environments,

computer-mediated prosthetics for military (and civilian) amputees, traumatic brain injury detection devices for soldiers, fused multiple-sensor night vision sensors, extremely high power lasers, and much more.

13. I have been recognized by the industry for my contributions to processor design. I received the Eckert-Mauchly Award in 2005 for "outstanding achievements in the design and implementation of industry-changing microarchitectures, and for significant contributions to the RISC/CISC architecture debate." The Eckert-Mauchly Award is generally viewed as the highest recognition in the field of computer architecture.

14. I was inducted into the National Academy of Engineering in 2006, the nation's highest honorary society for engineering achievement. In 2012, I was inducted into the American Academy of Arts and Sciences; other inductees in my "class" that year included Sir Paul McCartney, Hilary Rodham Clinton, and Mel Brooks. I am an IEEE Fellow.

15. In 2015, I received the Bob Rau Award from the IEEE, for "contributions to critical analysis of microarchitecture and the development of the Pentium Pro processor."

16. I have published many conference papers, sections of textbooks, and articles for magazines. I have also been named an inventor on 40 patents related to computer hardware and processor design. I have also been an editor for several Institute of Electrical and Electronics Engineers (IEEE) publications.

II. Materials Reviewed

17. In preparing this declaration, I have reviewed the specification, claims, prosecution histories of the Asserted Patents, and certain documents cited in the Asserted Patents and documents cited herein.

18. My opinions are based on these materials, as well as my knowledge and experience outlined above.

III. Legal Principles of Claim Construction

19. I am not an attorney. For the purposes of this declaration, I have been informed about certain aspects of the law that are relevant to forming my opinions. My understanding of the law is as follows.

20. Counsel has informed me that the claims of a patent define the scope of the alleged invention. Counsel has also informed me that the purpose of claim construction is to understand how a person of ordinary skill in the art (determined by the subject matter of the patent) would have understood the claim terms at the time of the alleged invention.

21. I understand that when construing a claim term, one looks primarily to the intrinsic patent evidence, including the words of the claims themselves, the patent specification, and the file history.

22. I also understand that extrinsic evidence, which is evidence external to the patent and the file history, may be useful in interpreting patent claims when the intrinsic evidence itself is insufficient.

23. I also understand that when a claim term has no generally accepted meaning to a person of ordinary skill in the art, the term's meaning must be found elsewhere in the patent. I further understand that such terms should be construed only as broadly as provided for by the patent itself.

IV. A Person of Ordinary Skill in the Art

24. It is my understanding that there is a dispute concerning the actual priority date of the Asserted Patents. ACQIS' infringement contentions state that the priority date of the '768, '750 and '797 patents is no later than May 12, 2000 and the priority date of the '654 and '140 patents is no later than May 14, 1999. *See* Plaintiff ACQIS LLC's Preliminary Infringement Contentions at page 6. Microsoft, however, asserts that the priority date of the '797, '768, and '750 patents is April 15, 2011 and the priority date of the '654 and '140 patents is November 10, 2011.

Defendant's Preliminary Invalidity Contentions and Disclosures and Subject Matter Eligibility Contentions at page 29.

25. In my opinion, based on the technology disclosed in the Asserted Patents, the level of skill of the person of ordinary skill in the art ("POSITA") would be the same regardless of which date is used as the priority date. Specifically, in my opinion, the relevant POSITA is a person who had at least a Master's Degree in electrical engineering, computer engineering, computer science, or a related subject, or a Bachelor's Degree in electrical engineering, computer science, or a related subject and three years of experience working with computer architecture, computer buses, and related technologies. I understand from counsel that ACQIS has used the following definition for the level of ordinary skill in past proceedings: "[A] person of ordinary skill in the art ("POSITA") concerning the technology described and claimed in the ACQIS patents-in-suit would have at least a bachelor's degree or the equivalent in computer or electrical engineering (or related academic fields) and three to four years of additional experience in the field of computer architecture, computer system design, or computer communication protocols, or a closely related area of endeavor, or an equivalent combination of education and experience." My opinions are the same under either level of skill of a POSITA.

26. Based on my professional experience, I have an understanding of the capabilities of a person of ordinary skill in the relevant field. Further, as detailed above, I myself qualify as at least a POSITA as of the earliest priority date of the Asserted Patents.

V. "PCI Local Bus Specification

27. Many claims of the Asserted Patents recite "Peripheral Component Interconnect (PCI) bus transaction" or "PCI bus transaction." *See* Defendant's (Microsoft) Disclosure Of Preliminary Claim Constructions at page 2; Plaintiff ACQIS LLC's Preliminary Claim Constructions at 1.

28. It is my understanding that ACQIS and the Defendants agree that these terms refer to "the industry standard PCI Local Bus Specification." *See* Defendant's (Microsoft) Disclosure Of Preliminary Claim Constructions at page 2; Plaintiff ACQIS LLC's Preliminary Proposed Claim Constructions at 1-2.

29. According to ACQIS, the priority date of the '768, '750 and '797 patents is no later than May 12, 2000 and the priority date of the '654 and '140 patents is no later than May 14, 1999. See Plaintiff ACQIS LLC's Preliminary Infringement Contentions at page 6. As of those dates, revisions 1.0, 2.0, 2.1 and 2.2 of the PCI Local Bus Specification had been released. *See* Ex. 45 (PCI Local Bus Specification Revision 2.2), Revision History Table:

REVISION	REVISION HISTORY	DATE
1.0	Original issue	6/22/92
2.0	Incorporated connector and expansion board specification	4/30/93
2.1	Incorporated clarifications and added 66 MHz chapter	6/1/95
2.2	Incorporated ECNs and improved readability	12/18/98

30. More specifically, revision 1.0 was released on June 22, 1992, revision 2.0 was released on April 30, 1993, revision 2.1 was released on June 1, 1995, and revision 2.2 was released on December 18, 1998. A POSITA would have understood that "the industry standard PCI Local Bus Specification" refers to those versions of the PCI Local Bus Specification because those were the only versions that existed at that time.

31. It is my opinion that a POSITA would have looked to all relevant sections of the PCI Local Bus Specification, and been capable of doing so, to understand what a transaction in accordance with "the industry standard PCI Local Bus Specification" means and requires to practice the relevant claims. With respect to the Asserted Patents, however, this would not include certain

sections, for example hardware sections such as the mechanical specifications for the PCI expansion card and connector, that are irrelevant to the PCI transactions contemplated by the Asserted Patents. *See* Ex. 45 (PCI Local Bus Spec. v. 2.2) at chapter 5.

32. The parties also agree that "Peripheral Component Interconnect (PCI) bus transaction" or "PCI bus transaction" should mean "a transaction, in accordance with" "the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component." *See* Defendant's (Microsoft) Disclosure Of Preliminary Claim Constructions at page 2; Plaintiff ACQIS LLC's Preliminary Proposed Claim Constructions at 1-2.

33. It is my understanding from Counsel that the Court of Appeals for the Federal Circuit ("Federal Circuit") has adopted that construction in an appeal decision in another litigation involving ACQIS and other patents related or similar to the Asserted Patents.

34. ACQIS, however, also alleges that the terms also include transactions "backwards compatible with the industry standard PCI Local Bus Specification." Plaintiff ACQIS LLC's Preliminary Proposed Claim Constructions at 1-2.

35. I disagree with ACQIS's construction. For starters, it broadens the claim term beyond what a POSITA would have understood at the time and beyond what the Federal Circuit held the term to mean. Specifically, ACQIS's construction improperly expands the construction to include a separate class of transactions not in accordance with, but only backwards compatible with, the PCI Local Bus Specification. That is, ACQIS's construction includes any transaction that is less than a complete transaction in accordance with the PCI Local Bus Specification. ACQIS's "backwards compatibility" insert allows it to allege that any transaction is a PCI bus transaction, despite differences in information transmitted and how it is transmitted.

36. In addition, by allowing transactions not in accordance with the PCI Local Bus Specification, Plaintiff's construction is contrary to, and not consistent with, the Federal Circuit's adopted claim construction.

37. Moreover, I do not see any evidence in the Asserted Patents that indicates a "PCI bus transaction" encompasses "backwards compatible" transactions that are not in accordance with the PCI Local Bus Specification. I note that the term "backwards" does not appear in any of the Asserted Patents, let alone the phrases "or backwards compatible with" or "backwards compatible" or anything equivalent. As such, a POSITA would have understood the claim term, consistent with the intrinsic evidence, to require an actual PCI bus transaction (i.e., "a transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component"), and not merely a "backwards compatible" transaction.

VI. USB Specification

38. Many claims of the Asserted Patents recite "Universal Serial Bus (USB) protocol" or "Universal Serial Bus (USB) protocol data/information." *See* Defendant's (Microsoft) Disclosure Of Preliminary Claim Constructions at page 2; Plaintiff ACQIS LLC's Preliminary Proposed Claim Constructions at 6.

39. It is my understanding that Defendants asserts that these terms mean "[data/information conveyed according to] the protocols defined in the Universal Serial Bus Specification Revision 2.0 and the prior versions of this standard." *See, e.g.,* Defendant's (Microsoft) Disclosure Of Preliminary Claim Constructions at page 2. ACQIS, on the other hand, asserts that the terms do not need construction. Plaintiff ACQIS LLC's Preliminary Proposed Claim Constructions at 6.

40. According to ACQIS, the priority date of the '768, '750 and '797 patents is not later than May 12, 2000 and the priority date of the '654 and '140 patents is no later than May 14, 1999. See

Plaintiff ACQIS LLC's Preliminary Infringement Contentions at page 6. As of those dates, revisions 1.0 and 1.1, and earlier revisions, of the Universal Serial Bus Specification had been released. More specifically, revision 1.0 was released on January 15, 1996 and revision 1.1 was released on September 23, 1998. *See* Ex. 46 (Universal Serial Bus Specification Revision 2.0), Revision History Table:

Scope of this Revision
The 2.0 revision of the specification is intended for product design. Every attempt has been made to ensure a consistent and implementable specification. Implementations should ensure compliance with this revision.

Revision History

Revision	Issue Date	Comments
0.7	November 11, 1994	Supersedes 0.6e.
0.8	December 30, 1994	Revisions to Chapters 3-8, 10, and 11. Added appendixes.
0.9	April 13, 1995	Revisions to all the chapters.
0.99	August 25, 1995	Revisions to all the chapters.
1.0 FDR	November 13, 1995	Revisions to Chapters 1, 2, 5-11.
1.0	January 15, 1996	Edits to Chapters 5, 6, 7, 8, 9, 10, and 11 for consistency.
1.1	September 23, 1998	Updates to all chapters to fix problems identified.
2.0 (draft 0.79)	October 5, 1999	Revisions to chapters 5, 7, 8, 9, 11 to add high speed.
2.0 (draft 0.9)	December 21, 1999	Revisions to all chapters to add high speed.
2.0	April 27, 2000	Revisions for high-speed mode.

41. It is my understanding that the original non-provisional application 09/569,758 (now U.S. Patent No. 6,718,415) in the family chain of the '750, '768 and '797 Patents was filed on May 12, 2000. That application includes a specific reference to "USB 2.0." *See* Ex. 47 (US Patent No. 6,718,415), col. 7, ll. 1-2 ("For example, the invention can use Gbit Ethernet 1394, and USB 2.0."); col. 7, ll. 13-16 ("The implementation is not restricted to Ethernet serial communication and can use other high-speed serial communication such as USB 2.0, and 1394."). As shown above, as of May 12, 2000, revision 2.0 of the Universal Serial Bus Specification had been released. *See* Ex.

46, Revision History Table. More specifically, revision 2.0 was released on April 27, 2000 while draft versions were prepared on October 5, 1999 and December 21, 1999. A POSITA would have understood that "Universal Serial Bus (USB) protocol" or "Universal Serial Bus (USB) protocol data/information" refers to version 2.0 of the Universal Serial Bus Specification and prior versions because those were the only versions that existed at that time.

42. It is my opinion that a POSITA would have looked to all relevant sections of the Universal Serial Bus Specifications, and been capable of doing so, to understand what these claim terms mean and require to practice the relevant claims. With respect to the Asserted Patents, however, this would not include certain sections, for example certain hardware sections of the USB specification are irrelevant to the USB transactions contemplated by Asserted Patents. See Ex. 46 (USB 2.0 Spec.) at 85-118 (cable and connector specifications).

43. ACQIS proposes a "plain and ordinary meaning" to the USB terms. Plaintiff ACQIS LLC's Preliminary Proposed Claim Constructions at 6. It is my opinion, however, that ACQIS' "plain and ordinary meaning" constructions improperly allow ACQIS to attempt to capture modern USB standards that are not disclosed in the Asserted Patents' specifications and that had not yet been developed. There is a significant technological difference between USB 2.0 (and earlier specifications) and USB 3.0 and later versions of the specifications (e.g., half-duplex to full duplex). Thus, to understand the scope of the claims, a POSITA would need to know which USB specification to use to interpret the claims. Also, at the time of the alleged invention, a POSITA could not have known with certainty the technological aspects of future specifications of the USB standard. Thus, the scope of the claims would be unknown if interpreted to cover future, non-existing versions of the standard. Here, around the time of the alleged invention, USB 2.0 was the standard and a POSITA reading the Asserted Patents would have understood that the USB

described in the specification referred to USB 2.0 or earlier versions and that the claimed "Universal Serial Bus (USB) protocol [data/information]" was conveyed in accordance with USB 2.0, or earlier, specifications.

44. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Respectfully submitted,

Date: May 18, 2023

Robert P. Colwell, Ph.D.

APPENDIX A

ROBERT P. COLWELL

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PORTLAND, OR 97229
503-629-9638
BOB.COLWELL@GMAIL.COM

PROFESSIONAL EXPERIENCE

- **Director**, Microsystems Technology Office, DARPA Arlington VA 2012-2014
- **Deputy Director**, Microsystems Technology Office, DARPA 2011-2012

  Led office of 17 program managers, budget ~$600M/yr, funding research on computer systems, nanophotonics, bioengineering, radar, comms, lasers, IR imaging, and much more.
- **Consultant**, Portland, OR 2001-2011, 2014 - present

  General computer HW/SW consulting to industry and academia (Safeware, the University of Pittsburgh, Intel, Qualcomm, venture capital companies, many startups, expert witness engagements, Lawrence Berkeley National Lab, US DoD)

- Named an **Intel Fellow** (27 Fellows in Intel's employee population of ~80,000) in 1997; winner of 2005 **Eckert-Mauchly Award**, highest award in field of computer architecture, for "outstanding achievements in the design and implementation of industry-changing microarchitectures, and for significant contributions to the RISC/CISC architecture debate"; elected to **IEEE Fellow** and **the National Academy of Engineering** in 2006 (the highest recognition in field of engineering) for "contributions to turning novel computer architecture concepts into viable, cutting-edge commercial processors." Inducted into the **American Academy of Arts and Sciences**, 2012. Winner of **IEEE Bob Rau Award**, 2015.

- **Chief IA-32 Architect**, Intel Corporation, Hillsboro OR, 1992-2001

  Lead IA32 architect, responsible for all of Intel's x86 Pentium CPU architecture efforts (direct management included 40 – 110 people): Pentium Pro, Pentium II, III, 4; Initiated and led Intel's Pentium 4 CPU development

- **Senior CPU Architect**, Intel Corporation, Hillsboro OR, 1990-1992

  One of three senior architects responsible for conceiving Intel's P6 microarchitecture, the core of the company's Pentium II, Pentium III, Celeron, Xeon, and Centrino families

- **Hardware Architect**, Multiflow Computer, New Haven, CT 1985-1990

  One of seven hardware engineers who created the world's first VLIW (very long instruction word) scientific supercomputer under direction of Josh Fisher

- **Hardware Engineer** (part-time) Perq Systems, Pittsburgh PA, 1980 - 1984

  Hardware design engineer working on graphics display hardware for first generation bit-slice-based engineering workstations

- **Member of Technical Staff**, Bell Telephone Laboratories, Holmdel, NJ, 1977-1980

  Hardware design engineer working on 8 and 32-bit microprocessors

EDUCATION

- **PhD in Computer Engineering**, Carnegie-Mellon University, 1985
- **MSEE** in Computer Engineering, Carnegie-Mellon University, 1978

- **BSEE** in Electrical Engineering, University of Pittsburgh, 1977

PUBLICATIONS

Wrote foreword to "Weaving High Performance Multi-Core Processor Fabric: Essential Insights to the Intel Quickpath Architecture", Maddox, Singh, Safranek, Intel Press 2009

National Research Council, The Future of Computing Performance: Game Over or Next Level?, Washington, D.C.: The National Academies Press, 2010.

VLIW: The Unlikeliest Architecture, IEEE Solid State Circuits News, 2009

Wrote intro to DE Shaw's article on the Anton molecular folding engine in CACM, July 2008

Contributed parameterized chapter 2 problem sets to Hennessy & Patterson's "Computer Architecture: A Quantitative Approach, 4th Edition" 2006

The Pentium Chronicles, IEEE/Wiley, December 2005

IEEE Computer Magazine, 48 columns for "At Random" column 2002-2005

Wrote foreword to Josh Fisher's book "Embedded Computing: A VLIW Approach to Architecture, Compilers and Tools", Morgan-Kaufman 2005

We May Need A New Box, IEEE Computer March 2004

Superscalar Processor Design, P6 chapter, Shen & Lipasti, McGraw-Hill 2003

Embedded Everywhere, National Academy of Science, October 2001

Intel's College Hiring Methods and Recent Results, Microelectronics Systems Education Conference, Robert Colwell, Gary Brown, Frank See, July 1999

Microprocessor, Wiley & Son Technical Encyclopedia, 1999

Challenges and Trends in Processor Design, roundtable discussion in IEEE Computer, January 1998

A 0.6um BiCMOS Processor with Dynamic Execution, Robert P. Colwell, Randy L. Steck, 1995 IEEE International Solid State Circuits Conference, pp. 176-177 (won best paper award)

Latent Design Faults in the Development of Multiflow's TRACE/200, 22nd Annual International Symposium on Fault-Tolerant Computing, Boston MA, July 1992

Architecture and Implementation of a VLIW Supercomputer, Robert P. Colwell, W. Eric Hall, Chandra S. Joshi, David B. Papworth, Paul K. Rodman, James E. Tornes, Proceedings of Supercomputing '90, New York, November 1990

A VLIW Architecture for a Trace Scheduling Compiler, Robert P. Colwell, Robert P. Nix, John J. O'Donnell, David B. Papworth, Paul K. Rodman, IEEE Trans. on Comp., V. 37, N. 8, Aug.1988

A VLIW Architecture for a Trace Scheduling Compiler, Robert P. Colwell, Robert P. Nix, John J. O'Donnell, David B. Papworth, Paul K. Rodman, Proceedings of the 2nd Int'l Conf. on

Architectural Support for Programming Languages and Operating Systems, Oct. 1987, Palo Alto CA (2021 Winner of Influential Paper Award from ASPLOS Conference)

Fast Object-Oriented Procedure Calls: Lessons from the Intel 432, Edward F. Gehringer, Robert P. Colwell, ISCA 13, June 1986, pp. 92-101

The Performance Effects of Architectural Complexity in the Intel 432, Robert P. Colwell, Edward F. Gehringer, E. Douglas Jensen, ACM Transactions on Computer Systems, Aug. 1988, V. 6, N. 3

A Display Architecture for Driving Two Different Bitmapped Displays from One Frame Buffer, Robert P. Colwell, 1st Int'l Conference on Computer Workstations, San Jose CA, November 1985

Computers, Complexity, and Controversy, R.P. Colwell, C.Y. Hitchcock III, E.D. Jensen, H.M. Brinkley Sprunt, C.P. Kollar, IEEE Computer, September, 1985, pp. 8-19

The Performance Effects of Function Migration and Architectural Complexity in Object-Oriented Systems, Robert P. Colwell, PhD thesis, Carnegie-Mellon University, Pittsburgh, PA, August 1985

Peering Through The RISC/CISC Fog: An Outline Of Research, Computer Architecture News, Vol. 11, No. 1, March 1983 pp. 44-50

A Perspective on the Processor Complexity Controversy, Proceedings of the International Conference on Computer Design, 1983, pp. 613-616

The Origin of Intel's Micro-ops, invited paper, IEEE Micro 2021

LECTURES AND INVITED TALKS

P6: Myths and Pipelined Realities, MP Forum '95 in Santa Clara

Evolution of Slot 1 and Slot 2, MP Forum '97 in Santa Clara

Micro '30 keynote speaker, 1997, San Jose

HPCA2 keynote speaker, Santa Clara, 1996

Talks on computing futures at CMU and Oregon Graduate Institute, Intel's Design Test and Technology Conference 1997-1998 (best presentation DTTC), invited keynote DTTC '04

LCPC (Languages and Compilers for Parallel Computing) keynote speaker, San Jose 1996

Intel Research Forum invited speaker, Hillsboro '96, Santa Clara '99

Intel Distinguished Lecture Series talks on the Pentium Pro at BYU, MIT, UCB, Stanford, CMU, Illinois, Wisconsin, Univ of Washington, OGI, UCLA

Distinguished Lectures: UC Davis May 2003; Carnegie-Mellon Univ Nov. 2003; USC April 2004

Microprocessor Report dinner speaker on Pentium Pro, March '95

Neural Networks for Computing Conference, Snowbird Utah, April 1994

IEEE Winter VLSI Workshop 1995

DARPA Winter PI conference, Pasadena CA, January 1994

International Applications Conference, San Diego CA, June 1994

Nature's Paradigm and the Challenge of Validation, Intel Validation Summit 1998, invited talk

Validation Lessons from Elsewhere, Intel Validation Summit 1999, invited talk

ISCA keynote, Anchorage Alaska, June 2002

ECE380 Seminar invited talk, Stanford Univ. February 2004

Invited speaker, Technology Management Lecture Series, PSU May 2004

Invited speaker, CSE Division Wide Seminar, University of Michigan, January 2005

Invited keynote speaker, IEEE Int'l Symp. on Async Circuits and Systems, NYC, March 2005

Invited speaker, IEEE Management Series, Portland OR, April 2005

Eckert-Mauchly Award acceptance speech, ISCA, Madison Wisconsin, June 2005

Invited keynote, International Multiconference on Computer Science and Computer Engineering, Las Vegas NV, June 2005

Invited speaker: Google, Sun Labs, Portland State University 2005

Invited speaker: Cadence, Carnegie-Mellon Univ. CS, Univ. of Rochester, Walla Walla College 2006

Invited keynote, PICMET, Portland Oregon, August 2005

Distinguished lecture, Univ. of Utah, March 2006

Invited speaker: Computer Science Symposium, St. Petersburg, Russia 2006

Invited speaker, IEEE-CS 60th anniversary meeting, Santiago Chile, San Diego CA 2006

Invited speaker, National Academies "Distinguished Voices" lecture series, April 2007, Irvine CA

Invited speaker, FCRC "Future Of Computer Architecture 2007", June, San Diego CA

Invited keynote speaker, ASAP 2007 conference, July, Montreal Canada 2007

Invited speaker, UC Irvine, "How To Be a Successful Engineer", Feb. 2008

Invited speaker, US Naval Workshop on Ship Design, Williamsburg, VA May 2008

Invited speaker, DARPA DSRC summer session, Santa Cruz CA July 2008

Distinguished Hopeman Lecture, Grove City College, April 2009

Many invited talks as DARPA MTO spokesperson on the end of Moore's Law 2011-2014

Invited speaker, Microsoft Research 20th Anniversary Symposium, Sept. 2011

Invited speaker, Computer Science and Telecommunications Board (CSTB), Sept. 2011

Invited speaker, Secretary of Defense Corporate Fellows, July 2012, 2013

Invited speaker after-dinner talk, Salishan Conference on High Performance Computing, April 2013

Invited speaker, Industrial Physics Forum, Baltimore MD, March 2013

Invited speaker, Computing Community Consortium (CCC), Pgh PA, March 2013

Invited speaker, National Defense University College, Wash. DC, May 2013

Invited speaker, Design Automation Conference, Austin TX, June 2013

Invited keynote, Hot Chips Conference, Stanford, August 2013

Invited speaker, Gov't Forum on Moore's Law, Wash. DC, November 2013

Invited talks at UT Austin, seminar & computer architecture lecture, November 2013

Invited speaker, Rebooting Computing, Wash. DC, December 2013

Invited speaker, Dartmouth College, January 2014

Invited speaker, MIT Annual Research Conference (MARC), January 2014

Invited speaker, Virginia Tech Univ., February 2014

Invited speaker, Univ. of Rochester, March 2014

Invited speaker, IEEE Technology Time Machine conf, October 2014

Invited speaker, DARPA HAPTIX kickoff meeting, Arlington VA, Nov. 2014

Invited speaker, CSTB Continuing Innovation in IT workshop, Washington DC, Mar. 2015

Invited keynote, Stanford SystemX "Headlights" Workshop, April 2015

Invited keynote, Berkeley Energy Efficient Electronics Systems Symposium, Oct. 2015

Invited speaker, University of Washington, Nov. 2015

Invited speaker, Arizona State University, Feb. 2016

Invited keynote, DoE Extreme Heterogeneity workshop, January 2018

Invited keynote, DARPA NICE workshop, Feb. 2018 (Neuro-Inspired Computing Elements), Oregon

Invited keynote, ModSim workshop, Seattle, August 2018

ECE Commencement speaker, Portland State University, June 2019

Member, National Academy of Engineering review panel for NIST (National Institute of Standards and Technology) Nanotechnology Division, June 2021

PANEL SESSIONS

DAC '91 panel session panelist; DAC '92 CAD tools workshop instructor

ICCD '91 moderator/organizer of panel session, San Jose CA

ICCAD-94, panel session panelist, November 1994, San Jose CA

Micro 26 '93, moderator/organizer of panel session, Portland OR

ISCA workshop talk, Santa Margerita Ligure, Italy 1995, panelist Phila. PA 1996

PAID 97 Workshop talk on "accidental performance decisions" with Dave Papworth

FPGA panel session panelist, November 1996, Monterey CA

ASPLOS-VII panel session panelist, October 1998, San Jose CA

IEEE Workshop on Low-Power design panel session, San Diego, CA 1999

Four panel sessions in 2000 at various conferences

Computer Research Assoc. "Grand Challenges" conference, Santa Cruz CA, Dec. 2005

DARPA MTO Exposition, Arlington VA July 2014

NSF Future Computing evaluation panel April 2018

ModSim 2018 panelist, Seattle WA

CONFERENCE COMMITTEES

ICCD 1990, 1991, 1992, 1993, 1994, 1995

IEEE Micro 24, 26, 27, 30, 31, 32, general co-chair 37, 39, 40, 41

ISCA 1999, 2000, 2008, 2009, 2010, 2015

Supercomputing 2013, 2014

TECHNICAL EXPERT LEGAL CASES WORKED

Intergraph v. Intel, 1998-2000, deposed twice

Techsearch v. Intel, 1999, deposed once

LGE v. Elonex, Morgan Lewis, ChathamLaw, Tom Nelson, 2002

Technical advice on PCI, memory system design

Intergraph v. Dell, Jones Day, Mark Ziegelbein, 2003-2004

Deposed, technical advice on buses, CPUs

Intergraph v. HP, Irell-Manella, Flavio Rose, 2004

Barbara Sales v. Intel, Brown Bain, Dan Bagatell, 2004

Fujitsu v. LG Electronics, Morrison Foerster, Alex Chartove, 2004

Opti v. NVIDIA, Cooley Godward, Tim Teter, 2004-2006

Expert reports for claims construction, invalidity/non-infringement

MEC/Acacia v. NVIDIA, Cooley Godward, Tim Teter, 2005

Kyocera v. Nokia, Jones Day, Keith Davis, 2005

Expert report for claim construction

HP v. Gateway, DLA Piper Rudnick Gray Cary, Alan Limbach, 2005

Expert report for claim construction, infringement contentions

Broadcom v. Qualcomm, Howrey, Vinay Joshi; DLA Piper, Dave Wiggins 2006

Expert reports for claim construction and non-infringement/invalidity, deposed twice, testified at trial, Orange County, Judge J. Selna

UniRAM v. Monolithic System Tech., Townsend & Townsend, George Schwab, 2006

EVE-USA v. Mentor Graphics, Cooley Godward, Brian Mitchell, Bill Galiani, 2006

Intergraph v. Toshiba, Foley Lardner, Stephen Lobbin, John Feldhaus, 2006-2007

Declaration re: Markman brief, expert report, deposed

MicroUnity v. Sony, Finnegan Henderson, Lei Mei, 2006-2007

Tech Property Limited v. NEC, Toshiba, Matsushita, Baker Botts, Michael Hawes, 2006-2007

Samsung v. Wistron, DLA Piper, Greg Lundell, Sal Lim, 2008 – settled

Expert reports for claim construction, infringement, rebuttals, deposed

Freescale v. ProMOS, Jones Day, Drexel Feeling, 2008 – settled

Expert report for infringement

ProMOS v. Freescale, Jones Day, Brent Ray, 2008 – settled

Expert report on non-infringement

Opti v. Nintendo, Cooley Godward, Tim Teter, 2008 – settled

SuperSpeed v. IBM, Jones Day, Mark Ziegelbein, 2008 – settled

Expert reports on non-infringement and invalidity, deposed twice

Saxon v. Nintendo, Cooley Godward, Matt Brigham, 2008

MOSAid v. NVIDIA, NVIDIA, Richard Calderwood, 2008

Opti v. Apple, Cooley Godward, Tim Teter, 2009

Expert reports on non-infringement and invalidity, deposed twice, testified at trial, Marshall Texas, Judge Everingham

Network-1 v. Cisco, Wilmer Hale, Joe Haag, 2009 – settled at trial July 2010

Claim construction declaration, expert report, deposed twice, testified at trial July 2010, Tyler, Texas; Judge L. Davis

Also represented Extreme Networks, Foundry, 3Com, Enterasys, and Adtran (all settled)

Samsung/LGE v. Kodak, Wilmer Hale, Joe Haag, 2009 expert report – settled

WARF v. Intel, Wilmer Hale, Jonathan Andron, James Quarles, 2009 – deposed; settled

ACQIS v. Sun/Oracle, DLA Piper, Alan Limbach, 2009

Expert report on non-infringement, deposed, settled January 2011

Xpoint v. Qualcomm, McDermott Will & Emery, Dave Dolkas – settled

Nokia v. Apple, Wilmer Hale, Joe Haag – settled

Alliacense v. SnapOn, McDonnell Boehnen Hulbert Berghoff, Brad Hulbert

Withdrew from case due to full time employment at DARPA 2011

Toshiba v. Wistron, Knobbe Martens Olson Bear, Reza Mirzaie – settled

Expert report on infringement, invalidity rebuttal, deposed

Panasonic v. Freescale, Jones Day, David Witcoff – settled

WARF v. Apple, Wilmer Hale, Bill Lee, Lauren Fletcher, Andrew Danford, 2014-2015

Invalidity expert report, damages expert report, deposed, testified at trial (7 hours), Madison WI, Judge William Conley

AVM v. Intel, Wilmer Hale, Lauren Fletcher, 2015-2017

Damages expert report, deposed, trial Wilmington DE May 2017

AST v. Texas Instruments, Covington Burling, Anupam Sharma, Hyun Byun, 2016

Invalidity expert report, case settled

AST v. Renesas, Foley Lardner, John Feldhaus, Pavan Agarwal, 2016

Invalidity expert report, case settled

PUMA v. Apple, Haynes Boone, David O'Brien, 2016

Invalidity expert reports, deposed twice, case settled

Futurelink v. Intel, Kirkland Ellis, Eric Cheng, 2014-2017

Invalidity, non-infringement expert reports, deposed 3 times, case settled

Broadcom v. Renesas, Morrison Foerster, Fahd Patel, Daniel Muino, 2018-2020

Invalidity, non-infringement expert reports, deposed twice, testified at ITC hearing

Semcon v. Amazon, Sidley Austin, Tung Nguyen, Cal Butcher, 2019

Invalidity expert report, deposed 8/15/19, case settled

VLSI Tech. v. Intel, Wilmer Hale, Christine Duh, George Manley, Jordan Hirsch, 2017-2021

Damages expert report, Rebuttal report, deposed twice

ACQIS v. Samsung, DLA Piper, Gianni Minutoli, 2021

Claim Construction declaration, deposed twice, case settled Dec. 2021

ACQIS v. Inventec, BlankRome, Greg Hermann, 2022

Damages & apportionment, case settled May 2022

Apple Inc. v. Future Link Systems, Inter Partes Review, EriseIP, Adam Seitz

IPR declaration filed, case settled April 2022

Apple Inc. v. Future Link Systems, Fish Richardson, John Brinkmann

Work on claim construction, case settled April 2022

Have served as confidential technical consultant on many other patent litigation matters involved CPUs, chipsets, buses, memories, electronics, design tools, video and other technologies.

OTHER

Selected as member of ISAT (Information Systems Advanced Technology) panel for DARPA, 2006-2009, co-chaired Machine Learning on Multicore 2009 with Carlos Guestrin and Greg Morrisett

Panelist, Dept of Defense Summer Study on Future Technology, summer 1999, Washington DC

CSTB Panelist, National Academy of Science, Networks of Embedded Processors, 1999-2000, Wash. DC

CSTB Panelist, National Academy of Science, Sustaining Growth in Computing Performance, 2006-2011, Wash. DC

IEEE Computer Magazine editor for High Performance Computing, 1995 to 1999

IEEE Computer Magazine editorial board member, Perspectives editor, 1999-present

Reviewer of dozens of technical books for Morgan Kaufmann, Mindshare, Addison-Wesley

Committee member on NSF funding for computer arch futures, Philadelphia, 1996

Intel Innovator's Day finalist '93, judge '95, judge '97

IEEE Senior Reviewer status in 1994, 1995, 1996 (conference papers, books, magazine articles)

Intel P6 public spokesman at dozens of radio, TV, and magazine interviews

Intel Divisional Award 1993 for DFA performance modeling tool

Intel Achievement Award 1996 for Pentium Pro Microarchitecture

CMU Alumni Merit Award, 1996, for technical leadership on Pentium Pro development

ACM Eckert-Mauchly award committee member, 1998-2001

Univ. of Pgh. Distinguished Alumni Award, 2000, for technical leadership on Intel's microprocessors

Univ. of Pgh. University Achievement Award, 2001, for accomplishments in field of Computing

Carnegie-Mellon Distinguished Alumni Fellows Award 2001

PICMET "Medal of Excellence" 2005

Judge for CSIDC (Computer Society Int'l Design Competition) 2005, 2006

Instructor ECE570, Adv. Computer Arch., Oregon State Univ., winter semesters 2000, 2003

Inventor or co-inventor on 40 patents